IN THE SPECIFICATION

Presented below are specification changes showing the changes made.

Please replace paragraph [0034] with the following amended paragraph:

[0034] **FIG. 3** shows an embodiment where MTX **200** of **FIG. 1** is represented by using two stage-0 scalable non-blocking switching networks **330** and **320** with M=Ma+Mb =10 conductors **301-310** composed of subgroups Ma = [A0-A4]=5 **301-305** conductors and Mb = [B0-B4]=5 **306-310** conductors. Each ~~Na~~Nb= 2 for the upper two input conductors of each of the four logic cells (composed of conductors **101-102** for cell **10**, conductors **105-106** for cell **20**, conductors **109-110** for cell **30** and conductors **113-114** for cell **40**) and ~~Nb~~Na= 2 for the lower two input conductors for each of the ~~k=~~four logic cells (composed of conductors **103-104** for cell **10**, conductors **107-108** for cell **20**, conductors **111-112** for cell **30** and conductors **115-116** for cell **40**). A full sized stage-0 scalable non-blocking switching network of **FIG. 3** would have (M-N+1)=10-4+1=7 program controlled switches per input conductor. Instead, in the embodiment of **FIG. 3**, the number of input switches is only four because of the separate Ma conductors and Mb conductors (with Ma=Mb=5) and the number N is broken into two parts (with Na=Nb=2). As such, the number of program controlled switches per input conductor in network **330** is Ma-Na+1=5-2+1=4 and the use of program controlled switches per input conductor in network **320** is Mb-Nb-1=4. While it is true that the Ma **301-305** conductors connecting to the ~~upper~~ lower two inputs of the four logic cells using network **330** maintain the connectivity illustrated in **FIG. 2** (and similar for Mb conductors **306-310** to the ~~lower~~ upper two inputs of the four logic cells using network **320**), it is not true that any arbitrary

use of [A0-A4], [B0-B4] to fan-in to the four logic cells is so. This constraint prevents arbitrary assignments of M conductors connecting to the N conductors through the two 0-SNs **320** and **330** of **FIG. 3**. However, the stage-0 scalable non-blocking switching networks **320** and **330** together can be an economic implementation to provide good connectivity for a programmable logic circuit while the software efforts in book-keeping and tracking the allowable M conductors usage are more complex than the scheme of **FIG. 2**. **FIG. 3** allows at least eight M conductors out of ten to be arbitrarily connected to the inputs of the four logic cells, where each one conductor connecting to one input to each of the four logic cells using networks **320** and **330**; the constraint here is that the ten conductors can not be arbitrarily assigned as in the **FIG. 2** case.